CLAIMS

1. A system for processing addresses having variable prefix lengths, the system comprising:

a plurality of content addressable memory (CAM) blocks, each configured to provide a hit signal and an index signal in response to an applied address;

a plurality of programmable storage elements configured to store a plurality of routing values;

a configurable switching circuit coupled to receive the hit signals from the CAM blocks and the routing values from the programmable storage elements, wherein the configurable switching circuit routes the hit signals in a first order in response to the routing values;

a priority encoder coupled to receive the hit signals routed by the configurable switching circuit, the priority encoder being configured to provide an output hit signal representative of an asserted hit signal having a highest priority in the first order;

a first multiplexer configured to route one of the routing values from the programmable storage elements as an index routing value in response to the output hit signal; and

a second multiplexer configured to route an index signal from one of the CAM blocks as an output index value in response to the index routing value.

2. The system of Claim 1, further comprising a static random access memory (SRAM) array, wherein the index routing value and the output index value are provided to access the SRAM array.

3. The system of Claim 2, wherein the SRAM array includes a plurality of SRAM blocks corresponding with the CAM blocks.

4. The system of Claim 1, wherein the configurable switching circuit comprises a plurality of multiplexers, each corresponding with one of the CAM blocks, and each being coupled to receive all of the hit signals from the CAM blocks.

5. The system of Claim 4, wherein each of the programmable storage elements is coupled to a corresponding one of the multiplexers, wherein each of the multiplexers routes one of the hit signals in response to the routing value stored in the corresponding programmable storage element.

6. The system of Claim 1, wherein one or more of the CAM blocks is designated to store only prefixes having a first length, and one or more of the CAM blocks is designated to store only prefixes having a second length, different than the first length.

7. The system of Claim 6, wherein one or more of the CAM blocks stores is designated to store only prefixes having a third length, different than the first and second lengths.

8. The system of Claim 6, wherein one or more of the CAM blocks are initially designated as spare CAM blocks that do not store prefixes unless one of the other CAM blocks becomes full.

9. The system of Claim 1, wherein the asserted hit signal having the highest priority and the output index value originate in the same CAM block.

10. The system of Claim 1, wherein the system includes thirty-two CAM blocks.

11. The system of Claim 1, wherein the addresses are Classless Inter-Domain Routing (CIDR) addresses.

12. The system of Claim 1, wherein a first set of the CAM blocks is designated to store a set of prefixes of a first priority chain, wherein each of the CAM blocks in the first set is designated to store a corresponding one of the prefixes of the first priority chain.

13. The system of Claim 12, wherein a second set of the CAM blocks is designated to store a set of prefixes of a second priority chain, wherein each of the CAM blocks in the second set is designated to store a corresponding one of the prefixes of the second priority chain.

14. The system of Claim 13, wherein the first set of the CAM blocks and the second set of the CAM blocks share a common CAM block.

15. The system of Claim 14, wherein the common CAM block stores prefixes having different lengths.

16. A method for processing addresses having variable prefix lengths, the method comprising:

storing prefixes having a first length in a first set of one or more content addressable memory (CAM) blocks;

storing prefixes having a second length in a second set of one or more CAM blocks, the second length being different than the first length;

receiving an input address with the first and second sets of CAM blocks;

generating a hit signal and an index signal with each of the CAM blocks in the first and second sets of CAM blocks in response to the input address;

storing a plurality of routing values in a programmable register;

routing the hit signal generated by each of the CAM blocks to a priority encoder in an order determined by the routing values;

generating an output hit signal with the priority encoder in response to the hit signals;

routing one of the routing values as an index routing value in response to the output hit signal; and

routing one of the index signals as an output index value in response to the index routing value.

17. The method of Claim 16, further comprising using the index routing value and the output index value to address a memory array.

18. The method of Claim 16, further comprising selecting the routing values such that the hit signals associated with the first set of CAM blocks are routed consecutively to the priority encoder, and the hit signals associated with the second set of CAM blocks are routed consecutively to the priority encoder.

19. The method of Claim 16, wherein the output hit signal is representative of an asserted hit signal having a highest priority.

20. The method of Claim 19, wherein the asserted hit signal having the highest priority and the output index value originate in the same CAM block.

21. The method of Claim 16, further comprising initially designating one or more CAM blocks as spare CAM blocks that do not store prefixes unless another CAM block becomes full.

22. The method of Claim 16, wherein the input address is a Classless Inter-Domain Routing (CIDR) address.

23. The method of Claim 16, further comprising:

storing prefixes having a third length, different than the first and second lengths, in a third set of one or more CAM blocks.

receiving the input address with the third set of CAM blocks; and

generating a hit signal and an index signal with each of the CAM blocks in the third set of CAM blocks in response to the input address.

24. A method for processing addresses having variable prefix lengths, the method comprising:

analyzing the addresses to identify a first priority chain having a first plurality of prefixes, and a second priority chain having a second plurality of prefixes;

storing the prefixes of the first priority chain in a

first set of CAM blocks, wherein each of the CAM blocks in the first set of CAM blocks stores one and only one of the prefixes of the first priority chain;

storing the prefixes of the second priority chain in a second set of CAM blocks, wherein each of the CAM blocks in the second set of CAM blocks stores one and only one of the prefixes of the second priority chain, and wherein the first set of CAM blocks shares at least one CAM block with the second set of CAM blocks;

receiving an input address with the first and second sets of CAM blocks;

generating a hit signal and an index signal with each of the CAM blocks in the first and second sets of CAM blocks in response to the input address;

storing a plurality of routing values in a programmable register;

routing the hit signal generated by each of the CAM blocks to a priority encoder in an order determined by the routing values;

generating an output hit signal with the priority encoder in response to the hit signals;

routing one of the routing values as an index routing value in response to the output hit signal; and

routing one of the index signals as an output index value in response to the index routing value.